

Implementation of High Performance Adaptive Binary Range Coder

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Abstract

Video or image compression is important for any multimedia applications. There are number of coders available for video or image compression techniques. The implemented Adaptive Binary Range Coder uses virtual sliding window for probability estimation. A new adaptive window size selection algorithm is used to improve the compression performance of encoder. In comparison with the binary range coder with a single window, the implemented algorithm provides a faster probability adaptation at the initial encoding and decoding stage, and more precise probability estimation for very low entropy binary sources. In this system virtual sliding window is used for probability estimation instead of look up tables, therefore the memory requirement is less as compared to previous system. The power consumption of implemented system is measured by the Xilinx Xpower analyser. The power consumption is reduced up to 21% in implemented Adaptive Binary Range Coder (ABRC) as compared to previous coders like MQ-coder.

Keywords

Image compression, Video compression, Range coding, Arithmetic coding, Entropy coding, FPGA, Verilog, HDL.

I. Introduction

The image and video compression plays an important role in various multimedia applications. For image and video compression encoder and decoders are used, like JPEG, JPEG2000, H.264 which is Advanced Video Coding (AVC) standard and H.265 which is High Efficiency Video Coding (HEVC) standard. In implemented adaptive binary range coder system computational complexity is considered as an important factor in video or image compression standards. In previous encoding systems, the computations cost has been much higher than the encoder system which uses lookup tables. Therefore, the fast Adaptive Binary Range Coder (ABRC) is implemented. The algorithm used in this system is adaptive window size selection algorithm which increases speed of the system. The virtual sliding window concept is important part of the adaptive window size selection algorithm. It allows to control the Tradeoff between the precision of probability estimation and the speed of probability adaptation. In this virtual sliding window, the window with small length provide a faster adaptation, but poor in a low probability estimation precision, and windows with longer length provide slower adaptation speed but it gives excellent estimation precision. If an short input binary sequence such as Akiyo which is low resolution video and Ballroom which is medium-resolution video then the probability adaptation speed is important and windows 2^5 and 2^6 gives the high performance. But if the input sequence is long such as Rush Hour which is high-resolution video like the probability estimation precision is most important and window size 2^8 provides the better performance. To achieve better compression performance, in implemented system adaptive window size selection algorithm is used. It uses small window lengths for a high-speed probability adaptation at the initial stage of the coding and for better probability estimation precision it switch to a longer window length. The total number of windows and their values used in this algorithm must be selected to achieve the better compression performance. There are four windows are used to enhance the compression performance. These four windows are $w=3, 5, 8, 10$ in that 2^5 is the main window. In this algorithm all the windows which are shorter than the main window which is 2^5 are used at the initial stage of the encoding for fast probability adaptation and for estimation of low probability long size windows are used. These four windows are operating

in parallel hence the speed of system is enhanced compared to the previous encoders.

II. Related Work

Video or image compression is important for any multimedia applications. There are number of coders available for video or image compression techniques. For image and video compression encoder and decoders are used, like JPEG, JPEG2000, H.264 which is AVC standard and H.265 which is HEVC standard. In implemented adaptive binary range coder system computational complexity is considered as an important factor in video or image compression standards. In previous encoding systems, the computations cost has been much higher than the encoder system which uses lookup tables. Therefore, the fast Adaptive Binary Range Coder (ABRC) is implemented. The algorithm used in this system is adaptive window size selection algorithm which increases speed of the system [1]. In implemented system the renormalization is byte renormalization hence the speed of system is faster as compared to other systems.

The technique presented in A low-complexity bit-plane entropy coding and rate control for 3-D DWT based video coding was fast video coding based on 3-D discrete wavelet transform (DWT). In this paper author proposes a novel low-complexity entropy coding of wavelet sub bands. For low entropy contexts It uses zero-run coder and ABRC for remaining contexts. author also propose efficient rate-distortion criterion to skip 2-D wavelet transforms. In this techniques the entropy coding is based on parent-child sub band tree. Finally, author propose virtual buffer concept based one pass rate control which is useful for adaptive Lagrange multiplier selection. This technique also gives 2 to 6 times less computational complexity compared to Advanced Video Coding standard (AVC)[3].

The technique presented in Rate-Complexity-Distortion Optimization for Hybrid Video Coding gives video encoding rate complexity-distortion optimization. Author proposes multi-scale and single-scale medium-granularity methods to achieve complexity control large dynamic range. Then dependent rate-distortion function based frame level complexity allocation developed. This technique uses reference searching algorithm for efficient utilization of computational block. Proposed algorithms

performance was verified by using Comprehensive simulation. The main target of RCDO is to achieve automatically the high performance in the form of compression for any platform and any complex input. By using these algorithms it will be more easy to maintain video codecs efficiently on any platforms.[4]
In terms of computational scalability and coding efficiency the proposed algorithm provides effective performance. For better coding efficiency the two rate distortion algorithms are combined.

III. Design Methodology

The adaptive binary range coder is implemented for video or image compression application. The system is based on the adaptive window size selection algorithm which enhance the speed of encoding. Adaptive binary encoding plays very important role in video and image compression, such as JPEG, JPEG2000, H.264 which is Advanced Video Coding(AVC), and H.265 which is High Efficiency Video Coding standard(HEVC). For implementation of effective hardware and software part great efforts are required.

A. Block Diagram

Fig. 1 shows block diagram of adaptive binary range coder system. The image or video input is given to MATLAB and the binary equivalent of same image or video is taken for encoding. The binary input which is equivalent to the image or video frame is given to the Isim simulator through the verilog coding. Isim simulator is simulator used in Xilinx tool. With the help of Xpower analyser the power consumption of encoder is measured.

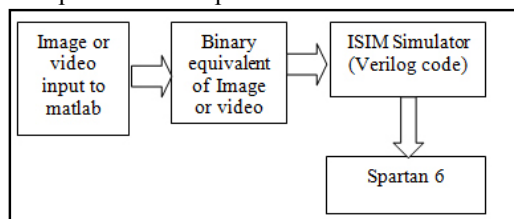


Fig.1 : System block diagram

The required memory in the form of LUTs or other blocks is calculated with the help of synthesis report.

B. General architecture of adaptive binary range coder

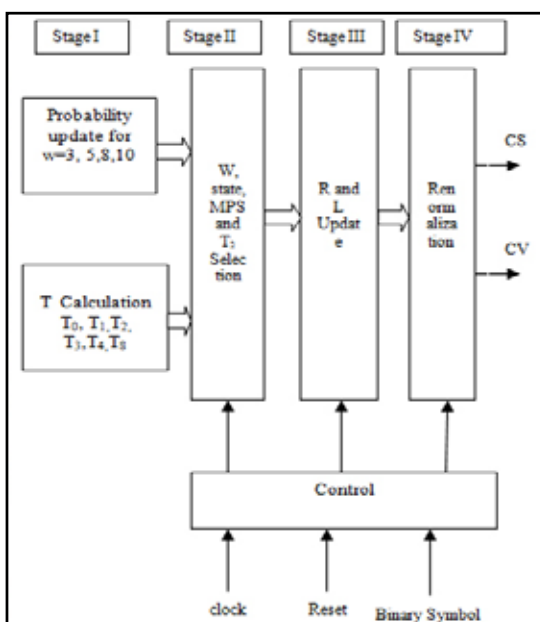


Fig.2 : General architecture of adaptive binary range coder

The general architecture of the implemented ABRC is shown in Fig.2. It consists of four stages. When reset is zero, the binary encoder receives binary data of image or video frame.

Initially the input bits are given to encoder, according to number of 1s and 0s the most probable symbols (MPS) are obtained. This process is in first stage of system where T calculations are necessary where T is the state of encoder. In this stage, the new probability values are calculated by using adaptive windows which are operating in parallel. In this stage present state of encoder and T_2 for the next binary symbol are calculated, the different six values of T generated by using T calculation circuit.

At the next stage, single value of T is selected from the six values which are generated by T calculation circuit. Depending on the size of window 2^w The value of T is selected.

At the third stage, The values of registers L , R and H are updated. Renormalization is very important for encoding system. At the last stage, According to upper eight bits of register L and H the renormalization is triggered. In implemented system the renormalization is byte renormalization hence the speed of system is faster as compared to other systems. After renormalization the 8 bit output which is code stream (cs) is generated.

IV. Results and Discussions

ABRC uses virtual sliding window (VSW) for estimation probability. To achieve better compression performance, here implemented a new adaptive window size selection algorithm. In case of renormalization, here byte renormalization is used which increases the speed of encoder? By adding a shifting networks after calculation for each internal variables which are used in adaptive Binary Range Coder (ABAC).

The input to the system is binary equivalent of image or video frame which is 8 bit. The tool used for implementation is Xilinx ISE 14.7 and MATLAB for binary equivalent of image or video frame.

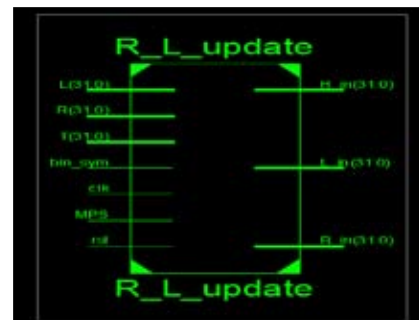


Fig. 3. RTL Schematic for L and R updates

Fig.3 shows RTL schematic of register L and R update. At each stage of encoding the register L and R are updated according to Most Probable Symbols (MPS) and state. The inputs for L and R update units are clock, MPS, Reset, Binary symbol.

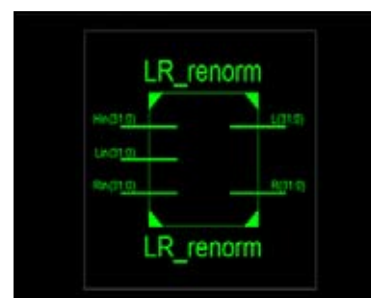


Fig. 4. RTL Schematic for Renormalization L and R variables

Fig. 4 shows the RTL schematic for renormalization unit. In implemented system the byte renormalization is performed for faster encoding.

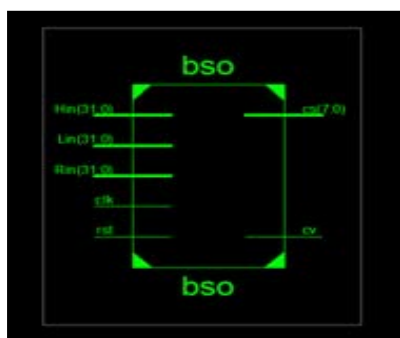


Fig. 5 : Bit Stream Output (BSO) RTL Schematic

The fig. 5 shows RTL schematic Bit Stream Output. The output of this unit is final output of the system. cv is code valid signal which used to indicates the valid output of system. cs is code stream which is final output of the system. Fig. 6 shows output of R and L update for given input

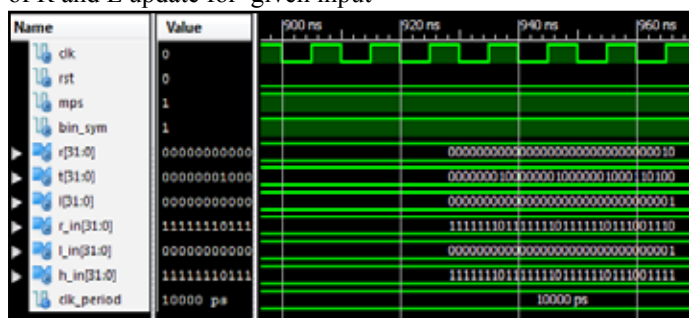


Fig. 6 : Rand L updated output for Given input

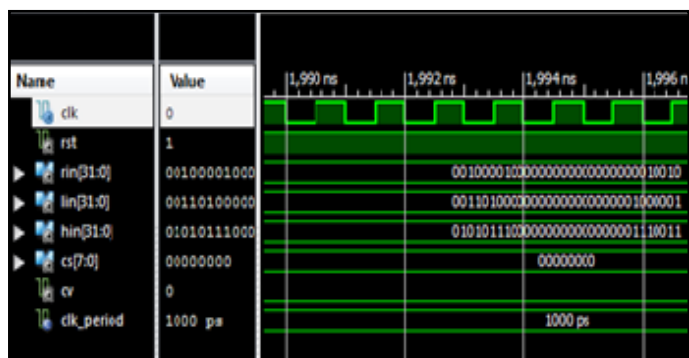


Fig. 7 : Bit stream output for different input combinations

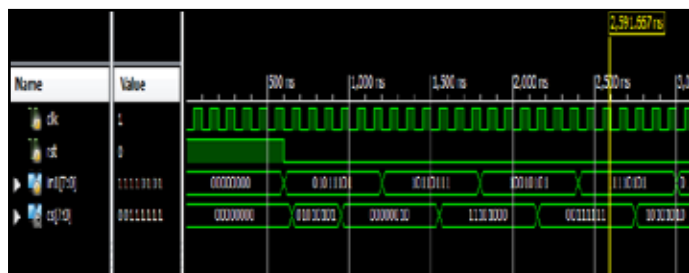


Fig. 8 : Output of ABRC for given Binary input

The simulated results shows that the 8 bit binary inputs are encoded with enhancing speed of encoding. The power consumption and memory requirement of encoder is also reduced in adaptive binary range coder. The simulation results are verified using MATLAB software.



Fig. 9 : Output verification using MATLAB

Fig. 9 shows MATLAB verification of ABRC. For input 01011101 we get output 00000010. Fig. 8 and Fig. 9 shows the Xilinx and MATLAB output are same for same input.

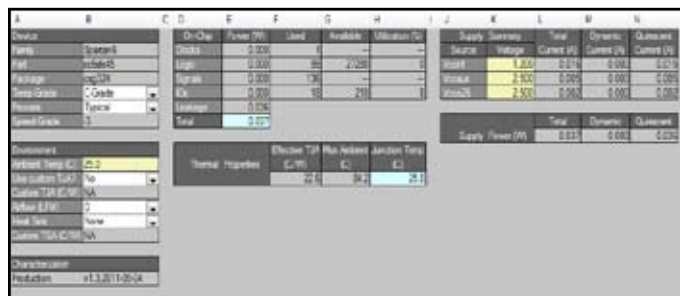


Fig. 10 : Power Consumption

Fig. 10 shows the power consumption of proposed system. By implementing this algorithm using Spartan 6 FPGA board the power consumption of system is reduced as compared to previous system.

Table I shows comparison of parameters of MQ coder[1] and ABRC on different platforms. According to Table I we can conclude that the Adaptive Binary Range Coder(ABRC) consumes less power and memory than MQ coder. The Implementation of ABRC on different platforms gives more advantages. The implemented system uses Spartan 6 FPGA platforms hence the implemented system will be more efficient for future image or video encoding standards.

Table 1 : Parameter Comparison of different coders

Parameters	MQ coder [1]	ABRC on Virtex 4	ABRC on Virtex 5	ABRC on Spartan 6
No of Slices (Memory)	6974	750	239	240
Power Consumption (mW)	1113.35	749.6	703	37
Clock Frequency (MHz)	48.30	105.92	125.29	100

V. Conclusions

In this paper A new efficient ABRC and its hardware architecture is proposed. In comparison with the previous M-coder and the MQ-coder, the proposed ABRC has a better compression performance in the case of video coding based on wavelet transform, It does not use additional memory such as lookup tables. Therefore, it can be more attractive for future high performance hardware image and video compression systems. In comparison with an ABRC with a single window, the proposed system provides a faster probability adaptation at the initial encoding decoding stage,

and more accurate probability estimation for very low entropy binary sources. Therefore, it can be more efficient and attractive for high performance encoding systems. The power consumption of system is up to 15.02mW, which is very less. Therefore, the implemented system can be more efficient for image and video compression.

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References

- [1] Evgeny Belyaev, Liu, Moncef, and YunSong Li, "An Efficient Adaptive Binary Range Coder and Its VLSI Architecture", *IEEE Transactions On Circuits And Systems For Video Technology*, Vol. 25, No. 8, August 2015.
- [2] E.Belyaev, "Adaptive window size selection for efficient probability estimation in binary range coder of the 3 D DWT video codec," in *Proc. 7th Int. Workshop Multiple Access Communication*, pp. 112–120, 2014.
- [3] Belyaev, E., Egiazarian, K., Gabbouj, M., "A low-complexity bit-plane entropy coding and rate control for 3-D DWT based video coding". *IEEE Transactions on Multimedia* pp, 1786–1799, 2013.
- [4] Li, X., Wien, M., Ohm, "Rate-Complexity-Distortion Optimization for Hybrid Video Coding", *IEEE Transactions on Circuits and Systems for Video Technology*, pp 957–970, 2011.
- [5] E. Meron and M. Feder, "Finite-Memory Universal Prediction of Individual Sequences" *IEEE Trans. Inform. Theory*, vol. 50-7, pp. 1506–1523, July 2004.
- [6] E. Meron and M. Feder, "Finite-Memory Universal Prediction of Individual Sequences" *IEEE Trans. Inform. Theory*, vol. 50-7, pp. 1506–1523, July 2004.