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Design and Realzation of FM0/Manchester Encoding for DSRC Application Using SOLS Technique

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Abstract
The dedicated short-range communication (DSRC) is Associate in Nursing rising technique to push the intelligent installation into our existence. The DSRC standards typically adopt FM0 and Manchester codes to succeed in dc-balance, enhancing the signal responsibleness. Still, the coding-diversity between the FM0 and Manchester codes seriously limits the potential to style a completely reused VLSI design for each. during this paper, the similarity-oriented logic simplification (SOLS) technique is projected to beat this limitation. The SOLS technique improves the hardware utilization rate from fifty seven.14% to 100% for each FM0 and Manchester encodings. The performance of this paper is evaluated on the post layout simulation in Taiwan Semiconductor producing Company (TSMC) zero.18-µm 1P6M CMOS technology. the utmost operation frequency is a pair of GHz and 900 rate for Manchester and FM0 encodings, severally. the facility consumption is one.58 mW at a pair of GHz for Manchester coding and one.14 mW at 900 rate for FM0 coding. The core circuit space is sixty five.98×30.43 µm2. The coding capability of this paper will totally support the DSRC standards of America, Europe, and Japan. This paper not solely develops a completely reused VLSI design, however additionally exhibits Associate in nursing economical performance compared with the prevailingworks.

Keywords
DSRC, FMO, Manchester,SOLS, Areacompact Retiming, Balance Logic Operation Sharing.

I. Introduction

Manchester committal to writing technique is a digital committal to writing technique within which all the bits of the binary information square measure organized in a specific sequence. Here a bit '1' is portrayed by transmittal a high voltage for [*fr1] length of the sign associated for future suspension amount an inverted signal can be send. once transmittal '0' in Manchester format, for the half cycle a low voltage can send, and for the next [*fr1] cycle a high voltage is send. The advantage of Manchester committal to writing is that, once causation a information having continuous high signals or continuous low signal (e.g.: 11110000), it's troublesome to calculate the quantity of one S and Os within the information. as a result of there's no transition from low to high or high to low for a specific period (Here it's four x T, T is that the time length for one pulse). The detection is feasible solely by hard the time length of the signal. however once we tend to code this signal in Manchester format there'll perpetually be a transition from high to low or low to high for every bit. so for a receiver it is simpler to find the information in Manchester format and also the likelihood for incidence of a blunder is incredibly low in Manchester format and it is a universally accepted digital cryptography technique

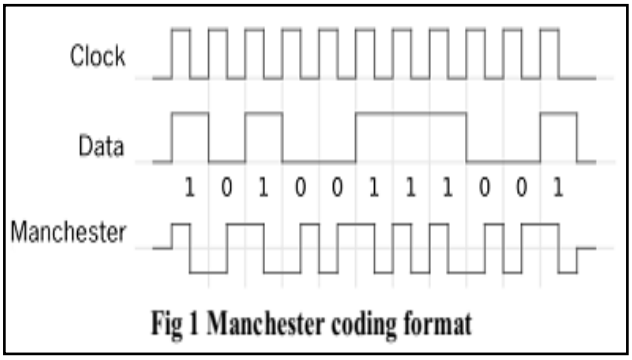

Fig 1 Manchester coding format

II. Literature Survey

The dedicated short-range communication (DSRC) could be a protocol for one- or two-way medium vary communication particularly for intelligent transportation systems. The DSRC is concisely classified into 2 categories: automobile-to-automobile and automobile-to-roadside. In automobile-to-automobile, the DSRC permits the message causing and broadcasting among vehicles for issues of safety and public info announcement [2], [3]. the security problems embrace blind-spot, intersection warning, put down cars distance, and collision-alarm. The automobile-to-roadside focuses on the intelligent transportation service, like electronic toll assortment (ETC) system. With ETC, the toll aggregation is electrically accomplished with the contactless IC-card platform. Moreover, the ETC is extended to the payment for parking-service, and gas-refueling. Thus, the DSRC system plays a crucial role in trendy industry. The system design of DSRC transceiver is shown in Fig. The higher and bottom components ar dedicated for transmission and receiving, severally. This transceiver is classed into 3 basic modules: micro chip, baseband process, and RF front-end. The micro chip interprets directions from media access management to schedule the tasks of baseband process and RF front-end. The baseband process is answerable for modulation, error correction, clock synchronization, and secret writing. The RF frontend transmits and receives the wireless signal through the antenna.

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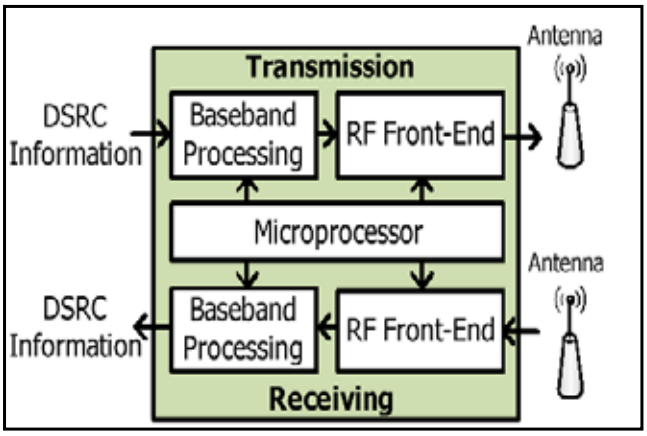


System architecture of DSRC transceiver

A. Review of VLSI Architectures for FM0 Encoder and Manchester Encoder

The projected VLSI design of Manchester encoder for optical communications. This style adopts the CMOS electrical converter and also the gated electrical converter because the switch to construct Manchester encoder. it's enforced by zero.35-µm CMOS technology and its operation frequency is one gigacycle. The literature more replaces the design of switch by the nMOS device. it's realised in 90-nm

CMOS technology, and also the most operation frequency is as high as five gigacycle. The literature develops a high-speed VLSI design nearly totally reused with Manchester and Miller encodings for frequence identification (RFID) applications. This style is realised in zero.35-µm CMOS technology and also the most operation frequency is two hundred rate. This hardware design is conducted from the finite state machine (FSM) of Manchester code, and is realised into field-programmable gate array (FPGA) prototyping system. the utmost operation frequency of this style is concerning 256 rate. The similar style methodology is more applied to singly construct FM0 and Miller encoders conjointly for radio frequency RFID Tag soul [8] . Its most operation frequency is concerning 192 rate. what is more, combines frequency shift keying (FSK) modulation and reception with Manchester codec in hardware realization

III. Coding Principles of fm0 code and Manchester code

In the following discussion, the clock signal and the input data are abbreviated as CLK, and X, respectively. With the above parameters, the coding principles of FM0 and Manchester codes are discussed as follows.

A. FM0 Encoding As shown in Fig. 2, for each X, the FM0 code consists of two parts: one for former-half cycle of CLK, A, and the other one for later-half cycle of CLK,B. The coding principle of FM0 is listed as the following three rules.

1) If X is the logic-0, the FM0 code must exhibit a transition between A and B.
2) If X is the logic-1, no transition is allowed between A and B.
3) The transition is allocated among each FM0 code no matter what the X is.

A FM0 coding example is shown in Fig. 3. At cycle 1, the X is logic-0; therefore, a transition occurs on its FM0 code, according to rule 1. For simplicity, this transition is initially set from logic-0 to -1. According to rule 3, a transition is allocated among each FM0 code, and thereby the logic-1 is changed to logic-0 in the beginning of cycle 2. Then, according to rule 2, this logic-level is hold without any transition in entire cycle 2 for the X of logic-1. Thus, the FM0 code of each cycle can be derived with these three rules mentioned earlier.

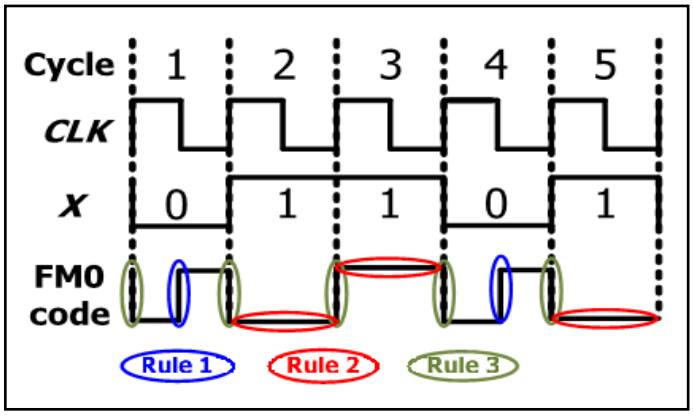


Illustration of FM0 coding example.

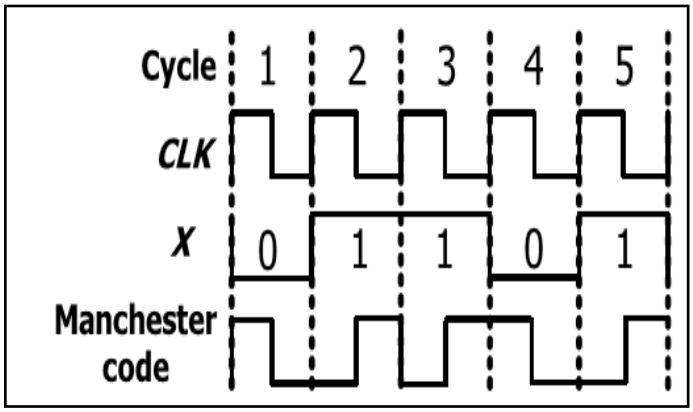
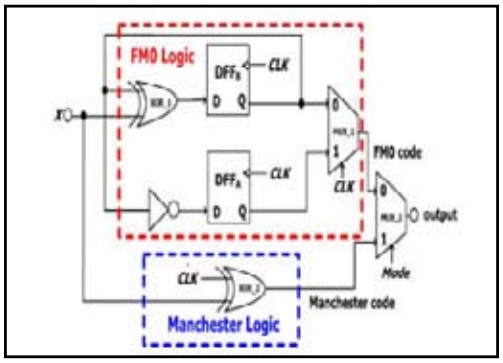


Illustration of Manchester coding example.

IV. Hardware Architecture of fm0 code and Manchester code

This is the hardware architecture of the fm0/Manchester code. the top part is denoted the fm0 code and then the bottom part is denoted as the Manchester code. in fm0 code the DFFA and DFFB are used to store the state code of the fm0 code and also mux_1 and not gate is used in the fm0 code. when the mode=0 is for the fm0 code. the Manchester code is developed only using the XOR gate and when the mode=1 is for the Manchester code. the hardware utilization rate is defined as the following

$$HUR = \frac{Active\ components}{total\ components} \times 100$$



Hardware architecture

The active components means the components are work in the both fm0 and Manchester code. The total components means the number of the components are present in the hole circuit. the HUR rate is given below the following section

TABLE-II

Coding	Active components(transistor count)/ total components (transistor count)	HUR
FM0	6(86)/7(98)	85.71%
MANCHESTER	2(26)/7(98)	28.57%
AVERAGE	4(56)/7(98)	57.14%

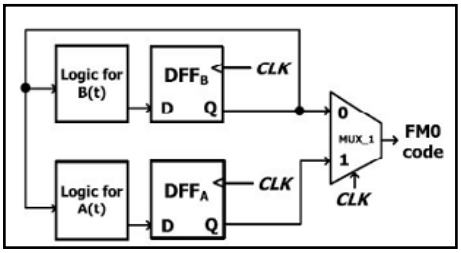
For both the encoding methods the total components is 7.for the fm0 code the total component is 7 and then the active component is 6.in Manchester code the total component is 7 the active component is 2.in both coding having 98 transistors are used without SOLS. The fm0 having 86 transistor, and then the Manchester having the 26 transistor. the average for both coding is 56 transistors .In proposed work reduce the total components from 7 to 6 and reduce the transistor counts. In this paper two multiplexer is used in proposed work reduce two multiplexer from one multiplexer, when reduce the multiplexer the total components are reduced the area and then the power consumption also reduced.

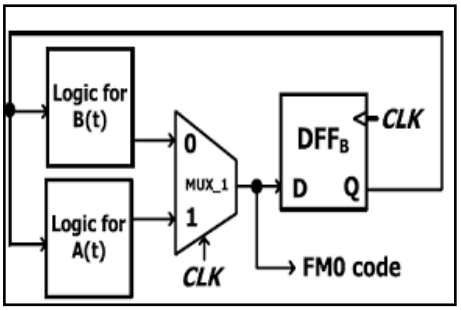
V. Hardware Architecture of fm0 code and Manchester encoder using sols coding

The SOLS technique is classified into two parts area compact retiming and balance logic operation sharing

A. Area compact retiming

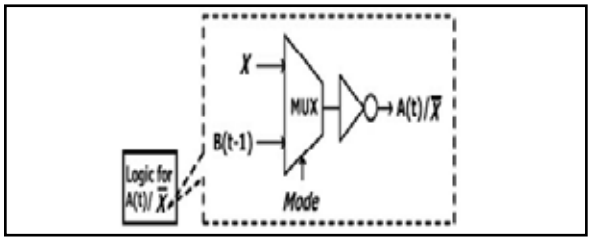
For fm0 the state code of the each state is stored into DFFA and DFFB .the transition of the state code is only depends on the previous state of B(t-1) instead of the both A(t-1) and B(t-1)





Area compact retiming FM0 encoding without area compact retiming.

The previous state is denoted as the A(t-1) and then the B(t-1).and then the current state is denoted as the A(t) and then the B(t).



FM0 encoding with area compact retiming.

Thus, the FM0 encoding just requires a single 1-bitflip-flop to store the previous value B(t−1).If the DFFA is directly removed, a non synchronization between A(t) and B(t)causes the logic fault of FM0 code. To avoid this logic-fault, the DFFB is relocated right after the MUX−1, where the DFFB is assumed be positive-edge triggered flip flop. At each cycle, the FM0 code, comprising A and B, is derived from the logic of A(t) and the logic of B(t), respectively. The FM0 code is alternatively switched between A(t) and B(t) through the MUX−1 by the control signal of the CLK. In the Q of DFFB is directly updated from the logic of B(t)with 1-cycle latency. when the CLK is logic-0, the B(t) is passed through MUX−1 to the D of DFFB. Then, the upcoming positive-edge of CLK updates it to the Q of DFFB. the timing diagram for the Q of DFFB is consistent whether the DFFB is relocated or not. the B(t) is passed through MUX−1 to the D of DFFB. Then, the upcoming positive-edge of CLK updates it to the Q of DFFB. the timing diagram for the Q of DFFB is consistent whether the DFFB is relocated or not. The transistor count of the FM0 encoding architecture without area-compact retiming is 72,and that with area-compact retiming is 50. The area-compact retiming technique reduces 22 transistors.

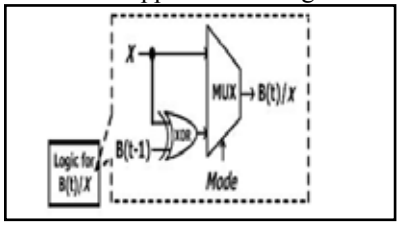
B. Balance logic operation sharing

The Manchester encoding is derived using the XOR operation. the equation of the XOR gate is given below.

X ⊕CLK=X CLK+~ X CLK

the concept of balance logic-operation sharing is to integrate the X into A(t) and X into B(t).the fm0 and Manchester logics have a common point of the multiplexer like logic with the selection of the CLK. the diagram for the balance logic operation sharing given the following.

The A(t) can be derived from an inverter of B(t − 1), and X is obtained by an inverter of X. The logic for A(t)/X can share the same inverter, and then a multiplexer is placed before the inverter to switch he operands of B(t − 1) and X. The Mode indicates eitherFM0 or Manchester encoding is adopted. The similar concept can be also applied to the logic for B(t)/X



Balance logic operation sharing

Nevertheless, this architecture exhibits a drawback that the XOR is only dedicated for FM0 encoding, and is not shared with Manchester encoding. Therefore, the HUR of this architecture is certainly limited. The X can be also interpreted as the X 0, and thereby the XOR operation can be shared with Manchester and

FM0 encodings, where the multiplexer irresponsible to switch the operands of B(t−1) and logic-0. This architecture shares the XOR for both B(t) and X, and there by increases the HUR. When the FM0 code is adopted, the CLR is disabled, and the B(t −1) can be derived from DFFB .Hence, the multiplexer can be totally saved, and its function can be completely integrated into the relocated DFF. The logic for A(t)/X includes the MUX−2 and an inverter. Instead ,the logic for B(t)/X just incorporates a XOR gate. In the logic for A(t)/X, the computation time of MUX−2is almost identical to that of XOR in the logic for B(t)/X. However, the logic for A(t)/X further incorporates an inverter in the series of MUX−2. This unbalance computation time between A(t)/X and B(t)/X results in the glitch to MUX−1,possibly causing the logicfault on coding. To alleviate this unbalance computation time, the architecture of the balan ce computation time between A(t)/X and B(t)/X The XOR in the logic for B(t)/X is translated into the XNOR with an inverter, and then this inverter is shared with that of the logic for A(t)/X. This shared inverter is relocated backward to the output of MUX−1. Thus, the logic computation time between A(t)/X and B(t)/X is more balance to each other.
The adoption of FM0 or Manchester code depends on Mode and CLR. In addition, the CLR further has another individual function of a hardware initialization. If the CLR is simply derived by inverting Mode without assigning an individual CLR control signal, this leads to a conflict between the coding mode selection and the hardware initialization. To avoid this conflict, both Mode and CLR are assumed to be separately allocated to this design from a system controller. Whether FM0 or Manchester code is adopted, no logic component of the proposed VLSI architecture is wasted. Every component is active in both FM0 and Manchester encodings. Therefore, the HUR of the proposed VLSI architecture is greatly improved.

Applications

- Parking-service
- Gas-refueling
- Modern automobile industry
- Short Range Communication

Advantages

The SOLS technique eliminates the limitation on hardware utilization by two core techniques: area compact retiming and balance logic-operation sharing. The area-compact retiming relocates the hardware resource to reduce the transistors.

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